REMARKS

Prior to entry of this paper, Claims 1-20 were pending. No amendments are made in this paper. Claims 1-20 are currently pending. For at least the following reasons, Applicants respectfully submit that each of the presently pending claims is in condition for allowance.

Claim Rejections

Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Sakai (JP 409063206) in view of Yasuda (JP 35906893), in further view of Castiglione et al. (U.S. Patent No. 7,079,616, hereinafter "Castiglione"), and in view of Davis (U.S. Patent No. 5,907,253), an in addition in view of Chang (US PG Publication 2002/0145478). Claim 3 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teaching as applied to Claim 1, and further in view of Jeon (US PG Publication 2003/0058053). Claims 4 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teaching as applied to Claim 1, and further in view of Prockup (US Patent No. 6,760,571). Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teaching as applied to Claim 1, and further in view of Watarai (US PG Publication 2003/0053577). Claims 8 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teaching as applied to Claim 1, and further in view of van Rassel (US Patent No. 4,697,277). Claims 8 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teaching as applied to Claim 1, and further in view of Bickley (US Patent No. 5,152,005). Claim 11 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teaching as applied to Claim 1, and further in view of Leung et al. (U.S. Patent No. 6,580,432, hereinafter "Leung"). Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teaching as applied to Claim 1. Each of the rejections is respectfully traversed.

Claim 1 is respectfully submitted to be allowable at least because there is no apparent reason to combine the proposed Sakai/Yasuda/Castiglione combination with Davis in the manner proposed by the Office.

The Office Action states that, "taking the combined teaching of Davis as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the accumulator circuit configured to provide a carry signal form the modulating waveform signal as taught by Davis so that the whole system would spend less time in an uncertain state and have less output signal phase noise." Applicants respectfully disagree. The alleged "advantages" of the combination only apply to fractional division. The proposed combination of Sakai/Yasuda/Castiglione does not employ fractional division. The Davis patent refers to certain advantages that the circuit of Davis has over prior art PLLs with fractional division, such as "the phase locked loop spending less time in an uncertain state which, in turn, results in less output signal phase noise". Davis discussed a method of fractional division in which the phase locked loop spends less time in an uncertain state than other prior art PLLs with fractional divisional. A PLL that does not use fractional divisional at all would not spend less time in an uncertain state by using the fractional division of Davis.

The proposed Sakai/Yasuda/Castiglione combination does not use fractional division, and therefore "the phase locked loop spending less time in an uncertain state which, in turn, results in less output signal phase noise" would not be a benefit enjoyed by the proposed combination. Accordingly, the references fail to provide an apparent reason for the combination of the proposed Sakai/Yasuda/Castiglione combination with Davis.

Additionally, there is no meaningful way to combine the proposed Sakai/Yasuda/Castiglione combination with Davis. In Castiglione, a modulator output is provided to divider 19a. In Davis, the carry output 127b of accumulator 126 is provided to fractional counter 122. There is no meaningful way to combine Sakai/Yasuda/Castiglione with Davis, since the circuitry alleged to be combinable are providing different, incomptable functions. The proposed combination would render Sakai/Yasuda/Castiglione unsuitable for its intended purpose.

Further, even if the proposed Sakai/Yasuda/Castiglione combination was combined with Davis, the combination would be for the output of the modulator 24 of Castiglione to go to 131a of FIGURE 6 of Davis, the integer information. There is no apparent reason to provide the modulation output signal of Castiglione to the accumulator of Davis. In Castiglione, the modulator output is provided to the divider to adjust the integer by which 18b is divided. If the references were

combined, then, the modulator output would go to input N (131a) of 122 of Davis, the integer information, not to the accumulator of Davis. Accordingly, the proposed combination does meet the limitations of Claim 1.

Claim 13 and 20 are respectfully submitted to be allowable at least for reasons similar to those stated above with regard to Claim 1. Claims 2-12 are respectfully submitted to be allowable at least because they depend from Claim 1. Claims 14-19 are respectfully submitted to be allowable at least because they depend from Claim 13.

CONCLUSION

It is respectfully submitted that each of the presently pending claims (Claims 1-20) are in condition for allowance and notification to that effect is requested. Examiner is invited to contact the Applicants' representative at the below-listed telephone number if it is believed that the prosecution of this application may be assisted thereby. Although only certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentable. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

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